Amendments to the Claims

The listing of claims will replace all prior versions, and listings of claims in the application.

Claims 1-19. (Cancelled).

Claim 20. (Previously presented) A method for manufacturing a clock generator that generates two non-overlapping clock signals, comprising:

providing an apparatus that includes a clock input portion, first and second clock outputs, a first feedback path for coupling said first clock output to said clock input portion, and a second feedback path for coupling said second clock output to said clock input portion;

determining if first and second clock signals generated by said first and second clock outputs, respectively, have clock edges that are non-overlapping for a predetermined time T;

adding one or more delay elements to said first and/or second feedback paths if said first and second clock signals do not have clock edges that are non-overlapping for said predetermined time T.

Claim 21. (Previously presented) The manufacturing method of claim 20, wherein adding a delay element to one of said first or second feedback paths comprises opening a first switch and closing a second switch along said first or second feedback path.

Claim 22. (Previously presented) The manufacturing method of claim 21, wherein said opening of said first switch and said closing of said second switch comprises performing fuse/anti-fuse processing.

Claim 23. (Previously presented) The manufacturing method of claim 21, wherein said opening of said first switch and said closing of said second switch comprises performing laser burning.

Claim 24. (Previously presented) The manufacturing method of claim 21, wherein said opening of said first switch and said closing of said second switch comprises performing ion beam milling.

Claim 25. (Currently amended) A method for manufacturing a clock generator that generates two non-overlapping clock signals, comprising:

providing an apparatus that includes a clock input portion, first and second clock outputs, a first feedback path for coupling said first clock output to said clock input portion, and a second feedback path for coupling said second clock output to said clock input portion;

determining if first and second clock signals generated by said first and second clock outputs, respectively, have clock edges that are non-overlapping for a predetermined time T; and

removing one or more delay elements from said first and/or second feedback paths if said first and second clock signals do not have clock edges that are non-overlapping for said predetermined time T.

Claim 26. (Previously presented) The manufacturing method of claim 25, wherein removing a delay element from one of said first or second feedback paths comprises closing a first switch and opening a second switch along said first or second feedback path.

Claim 27. (Previously presented) The manufacturing method of claim 26, wherein said closing of said first switch and said opening of said second switch comprises performing fuse/anti-fuse processing.

Claim 28. (Previously presented) The manufacturing method of claim 26, wherein said closing of said first switch and said opening of said second switch comprises performing laser burning.

Claim 29. (Previously presented) The manufacturing method of claim 26, wherein said closing of said first switch and said opening of said second switch comprises performing ion beam milling.